SXGA120 Rev 4 - Rev5 Design Comparison

This note focuses on the SXGA120 Rev5 design revision and the changes with respect to register settings and general operation compared to the SXGA120 Rev4 part. The Rev5 device was introduced in 2015 and contains updates to known deficiencies of the Rev4 design which dates back to the 2008 timeframe, as well as several performance upgrades. At the same time the Rev5 design maintains backward compatibility for optical, electrical and mechanical parameters with the Rev4 part to ease the transition to the new part for existing customers. In this note the differences between the two versions are explained and the opportunities for exploiting the performance improvements in the Rev5 part are described.

The backward compatibility allows Rev4 displays to be replaced with Rev5 parts with no changes to existing drive boards firmware and/or software to achieve similar performance (with one possible exception if the software/firmware does a Status register read check, since each version has a different number). However, enhancements to the Rev4 drive software would be required to unlock the additional features and performance benefits of the Rev5 version.

1 Rev5 Performance Enhancements

1.1 Elimination of stuck-on defects

To a varying degree all displays are susceptible to two types of defects – stuck-on and stuck-off pixels. A stuck-on defect is defined as a sub-pixel that is permanently fixed to an emitting state, even when the data calls for it to be off. Generally, this type of defect is not acceptable to users so only product with nearly zero stuck-on defects can be shipped to customers. Due to a modification of the pixel circuit and an optimization of the silicon backplane technology, the Rev5 displays have been found to be virtually free of the stuck-on defect as compared to its Rev4 counterpart.

1.2 Improved startup behavior and dimming control

To ensure proper startup and stabilization of the Rev4 display a software-defined power-on sequence has to be provided by the customer as part of their drive board design. For similar reasons, the rate at which dimming levels can be changed must be limited in the customer's software as well. The Rev5 design is much more reliable during startup as it does not depend on accurate timing of control registers by the user for power-on sequencing. Also, in Rev5 the dimming levels can be switched between any two values without regard to level differences or timing restrictions.

1.3 Option for 1.8V supply operation in addition to 2.5V

The Rev5 design includes an on-board linear regulator that allows it to operate from either a 2.5V supply just like the Rev4 version, or from a reduced supply voltage of 1.8V in order to simplify the system design and to potentially reduce power consumption. The 1.8V supply may be more compatible with the rest of the system hardware and as a result can eliminate the need for a separate 2.5V power supply when using the Rev5 part.

1.4 Eliminated requirement for system clock in order to operate I^2C serial interface

In the Rev4 design an active SCLK (system clock) signal is required for the I^2C interface to be operational. In the Rev5 design an active external SCLK signal is NOT required for the I^2C interface to be operational.

1.5 New power routing for improved image uniformity

Global display uniformity is affected by the distribution of power to the pixel array within the backplane. In order to further improve the global uniformity beyond the Rev4 specification, especially at the higher luminance levels, the power routing in the Rev5 design has been enhanced.

1.6 Greatly reduced dependency of luminance on 5V supply variation

In the Rev4 design there is a strong dependency of output luminance on the variation of the 5V supply. Typically the luminance decreases by about 10% for a 2% increase in the 5V supply. The Rev5 design mostly eliminates this dependency with a luminance change of less than 0.4% for a 2% increase in 5V supply.

2 Backward Compatibility with Rev4

2.1 Optical compatibility

Both versions of the display are identical in die size, display area, and the viewing area location.

2.2 Electrical compatibility

The Rev5 display if fully backward compatible with the Rev4 version with regards to the electrical interface specifications and the supply voltage requirements. In addition, the Rev5 will support an extended supply operating range as described below in section 3.5.

2.3 Register compatibility

The registers in the Rev5 design are a superset of the existing Rev4 register set, with the first 18 register definitions (00 to 17h) being identical for both types. Also the recommended startup values for the common registers are the same, except for the register 00 which provides the silicon revision number, and the temperature calibration registers (TREFDIV and TREFOFF) which are silicon process dependent and therefore have different optimal setting values. The Rev5 part has extra registers extending from address 18h to 23h which are used for controlling the additional functionality provided in the Rev5 design. By default these extra registers will initialize to provide the same operation as the Rev4 display.

Table 1 shows the recommended values for the register set that is common for both the Rev4 and Rev5 versions. The differences between them as described above are highlighted in yellow.

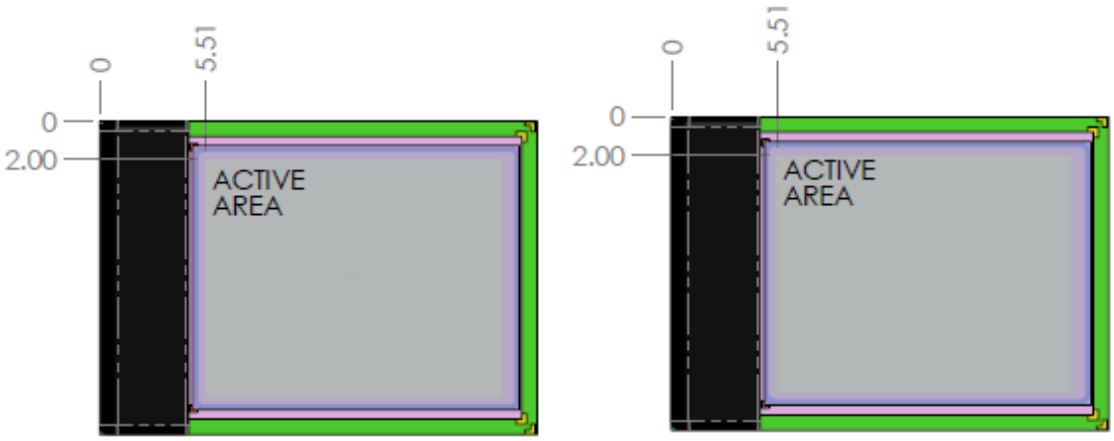
Table 1: Rev4 and Rev5 common register set

Register # (h)	Name	Rev 4	Rev 5
		Recommended Values	Recommended Values
00	STAT	00	05
01	VINMODE	03	03
02	DISPMODE	00	00
03	TOPPOS	06	06
04	BOTPOS	06	06
05	RAMPCTL	10	10
06	RAMPCM	44	44
07	DAOFFSET	50	50
08	EXTRAMPCTL	20	20
09	PWSAVE	00	00
0A	BIASN	02	02
0B	GAMMASET	0F	0F
0C	VCOMMODE	00	00
0D	VGMAX	0D	0D
0E	VCOM	70	70
0F	IDRF	30	30
10	DIMCTL	64	64
11	TREFDIV	1E	19
12	TEMPOFF	88	9A
13	TUPDATE	FF	FF
14	TEMPOUT	-	-
15	PWRDN	00	00
16	TPMODE	00	00
17	ANATEST/RESV	44	44

2.4 Mechanical compatibility

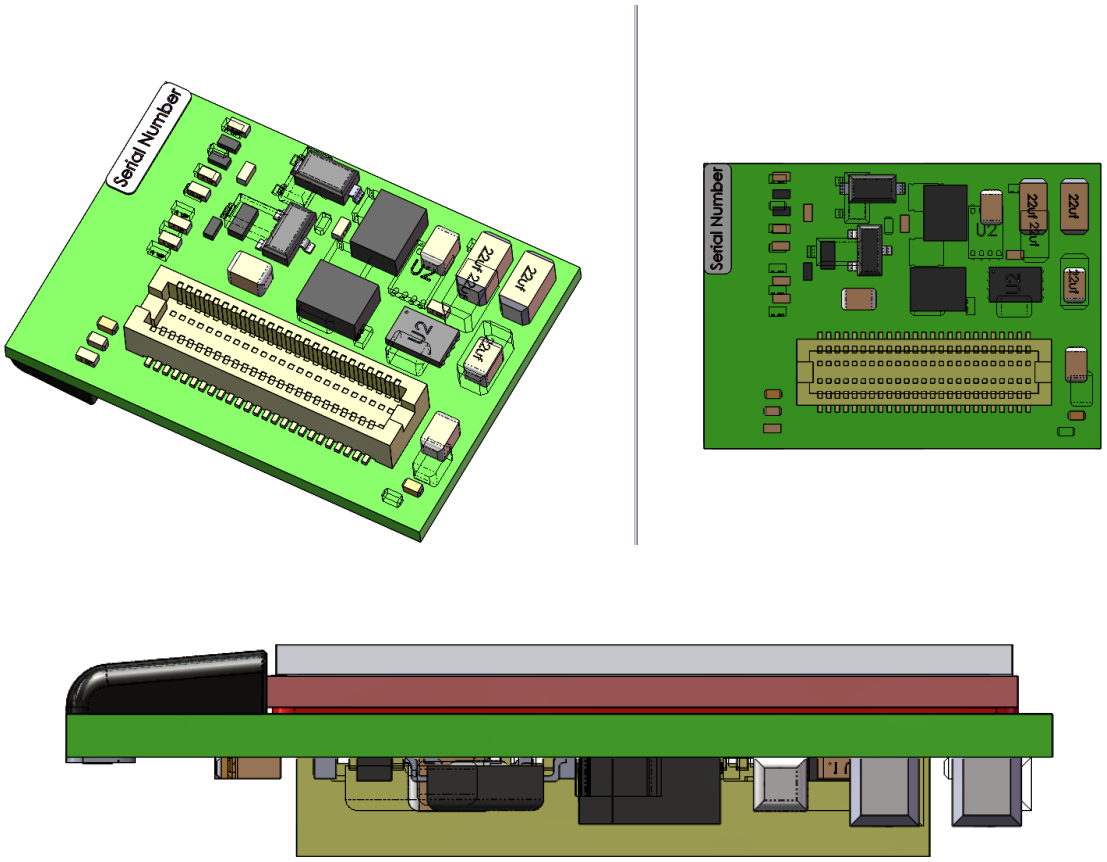
2.4.1 Front Side

There are no differences for the mechanical dimensions at the die attach side of the package. The die active area, glass lid or other optical element, and wirebond encapsulant are identical. (See the front views for both versions in the figure below.)

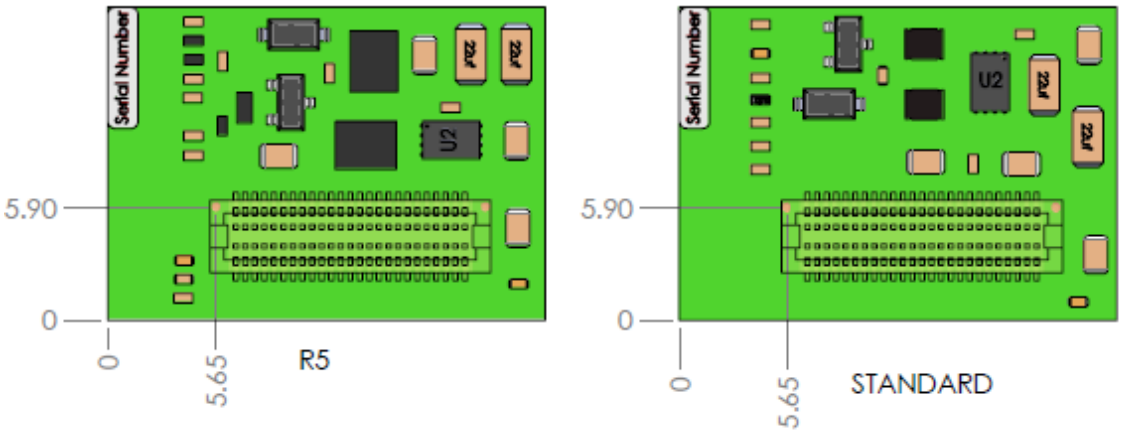


2.4.2 Rear Side

At the back plane, there are different discrete components positioned around the identically positioned connector J1. The differences are highlighted below with the R4 unit shown in wireframe on top of the R5 in shaded view.



Shown below is the rear view of the carrier boards side by side.



3 New Functionality in Rev5

3.1 Additional registers are in unused addresses

Both the SXGA120 Rev4 and the SXGA120 Rev5 types have the control registers ranging from address 00 through 17h in common. For the Rev5 design additional registers have been added for the address space from 18h to 23h specifically to control the new functionality in that design. If these are left unwritten after startup the Rev5 functionality will default to the Rev4 case.

Table 2 shows the extra control registers contained in the Rev5 design. The use of some of these is described below and additional detail can be found in the Rev5 datasheet.

Table 2: Extra registers in the Rev5 design

Register # (h)	Name	Rev 5
		Recommended Values
18	ROWRSTL	00
19	ROWRSTH	00
1A	VCOMCTL	3D
1B	NVCK0	99
1C	NVCK1	99
1D	LDOCTL	03
1E	FLTCTL	00
1F	FTLFLG	00
20	NPIXL	0C
21	NPIXH	05
22	NLINL	00
23	NLINH	04

3.2 Row Duty Rate Control

The Row Duty rate control function has been added to the Rev5 version. The duty rate for a row of data is defined as the fraction of a frame period during which the pixels will maintain a programmed value; for the remainder of the frame period the pixels will be driven to black. More details on this feature can be found in section 9.3.3 of the SXGA120 Rev5 datasheet. The new ROWRESET registers (18h and 19h) are used to set the desired duty rate.

3.3 Improved VCOM generator

The Rev4 design includes an on-board voltage converter that is used to generate a negative supply (VCOM) for biasing the OLED pixel array. This converter is also used to control the overall luminance of the display through register settings (IDRF and DIMCTL). To ensure proper startup and stabilization of the display a software-defined power-on sequence has to be provided by the customer as part of their drive board design. For similar reasons, the rate at which dimming levels can be changed must be limited in the customer's software as well. In contrast, the Rev5 VCOM generator includes hardware-based soft-start and current sensing functionality that relieves the customer of any control limitations during the power-on sequence and dimming level change. As a result, the large step-change limitation described in section 9.4.4 and power-on sequence described in section 9.7 of the Rev4 datasheet do not apply for the Rev5 design. Unlike the Rev4 display in which the IDRF level should be incremented by steps of no more than 1h per I^2C write command, the Rev5 level can be switched between any two levels with one I^2C instruction.

Registers 1Ah through 1Ch have been added to facilitate additional control options for the VCOM generator.

3.4 Separate external resistors for IDRF and BIASN control

External resistors Rext_idrf and Rext_vtn (125Kohm nominally) are used to separately adjust the IDRF and BIASN current. This allows for an extended brightness control range, particularly at low brightness levels where the Rev4 design tends to be susceptible to noise and instability. A new register (P_Biasn<2:0>) has been added to enable software control of the BIASN current according to the relation I(biasn) = (Vbg / Rext_vtn / 1000) * P_Biasn<2:0>.

3.5 On-chip 1.8V LDO regulator

The Rev5 design includes a Low-Drop-Out (LDO) linear regulator on-chip to permit operation from either the 2.5V supply as required by the Rev4 display or with a 1.8V supply. The lower supply voltage is more likely already available in the drive board due to requirements from other microelectronic components, and as a consequence the Rev5 display could result in a simpler system by dispensing with the need for a separate 2.5V power supply. A 3 bit register, LDO_CTL<2:0> at address 1Dh, has been added for fine tuning the LDO output level.